ADS Application Notes

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Impedance Matching Network Design for Amplifier to meet Gain, Input Reflection Coefficient and Stability Requirements

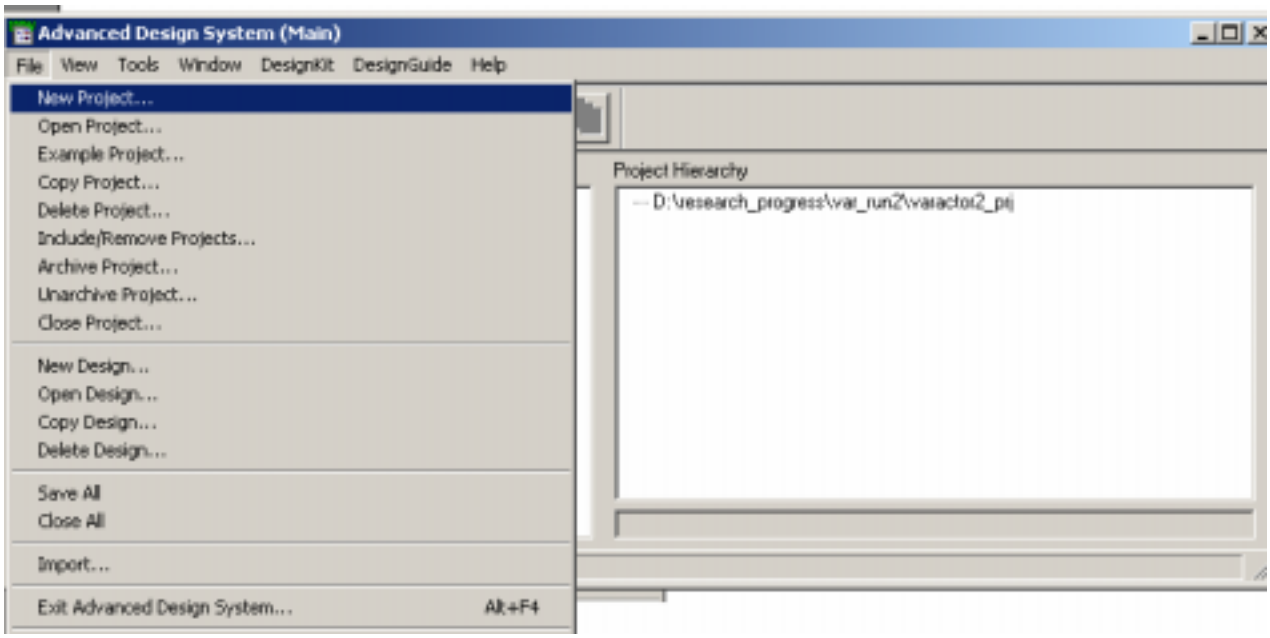
Introduction

This application note describes the procedure of designing the input matching network for amplifier to fulfill specific gain, input reflection coefficient and stability requirements. With the idea of conjugate matching, minimum signal reflection will occur at the input port of an amplifier and this will result in small reflection coefficient and larger gain. It is also important to make sure the amplifier is operating in stable region and oscillation will not occur.

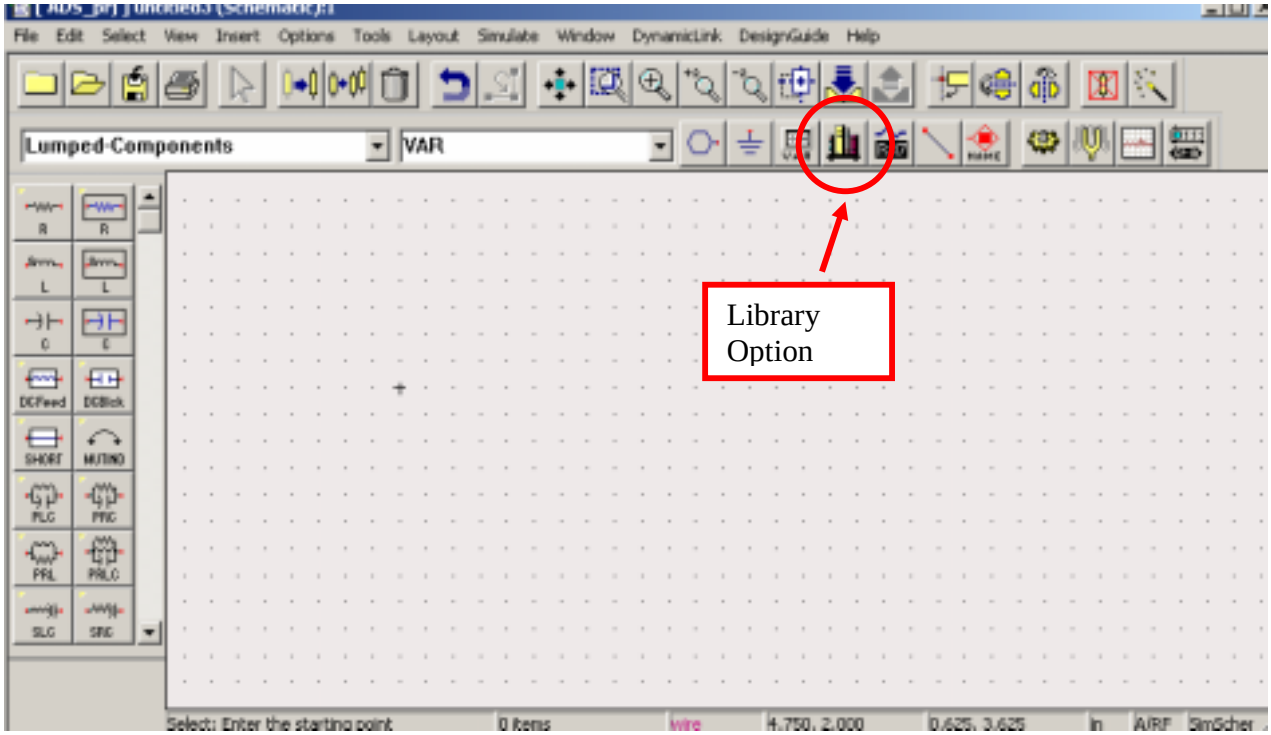
Design procedures

Before designing the input matching network for the amplifier to fulfill the gain and oscillation requirements, an appropriate biasing circuit is needed to make the transistor operate proper condition. Afterwards, effort will be paid on design a proper input matching network to reduce the input signal reflection at the input interface of the amplifier. The detailed procedures to design the biasing circuit and input matching network are shown below step by step.

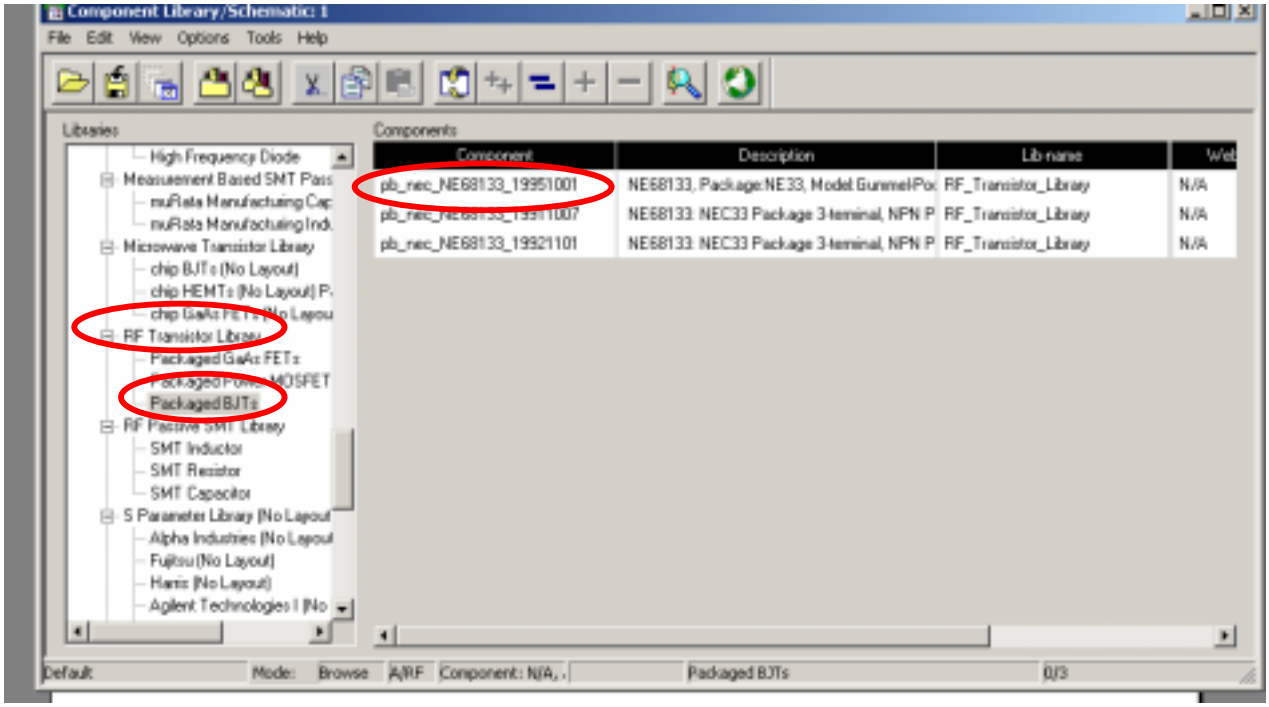
1. Open ADS program. Choose "File → New Project" to open a new project.



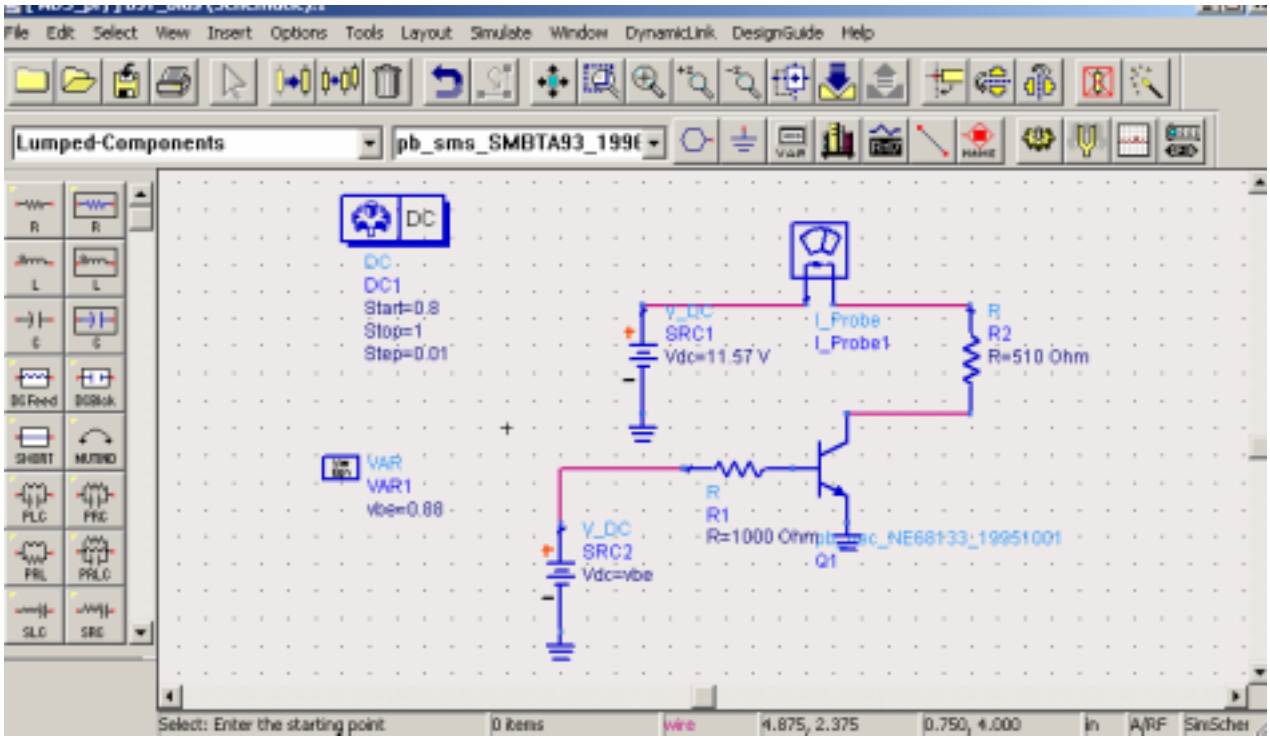
2. In the new schematic of the project, push the "Library" button to open a library lists to choose the suitable transistor model to build the amplifier.



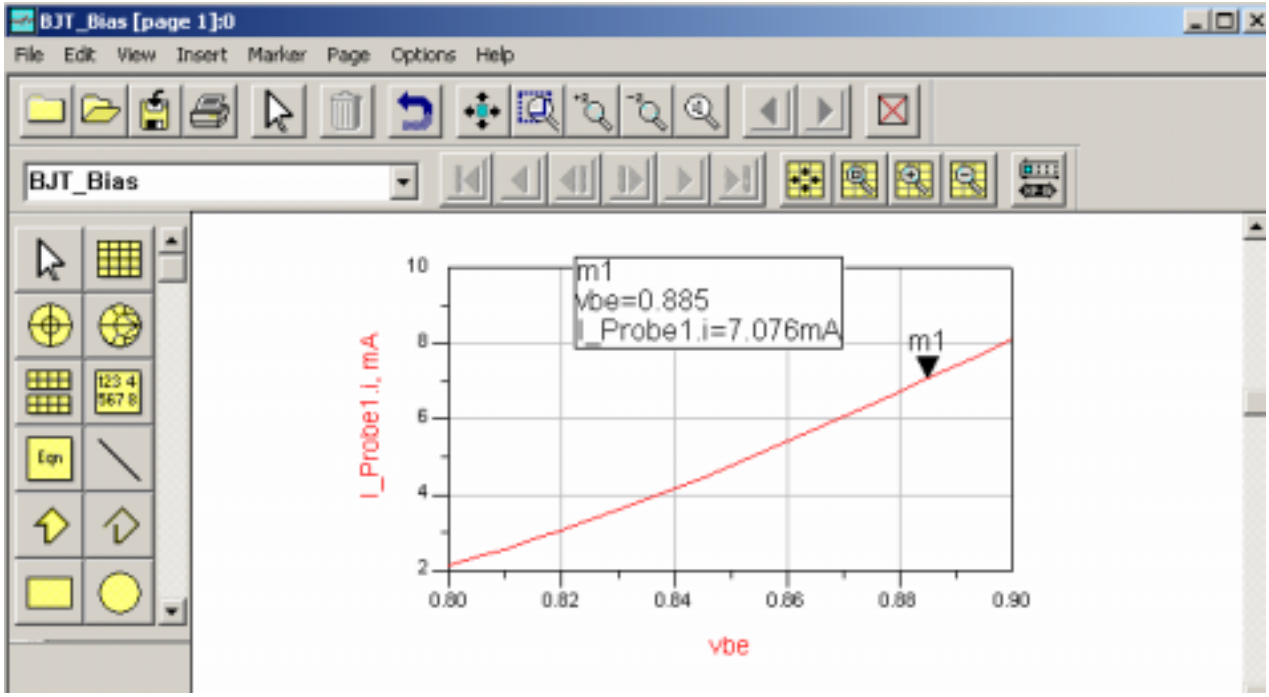
3. After opened the Library List window, choose "RF Transistor Library → Packaged BJTs" to choose the transistor pb_nec_NE68133_19951001.



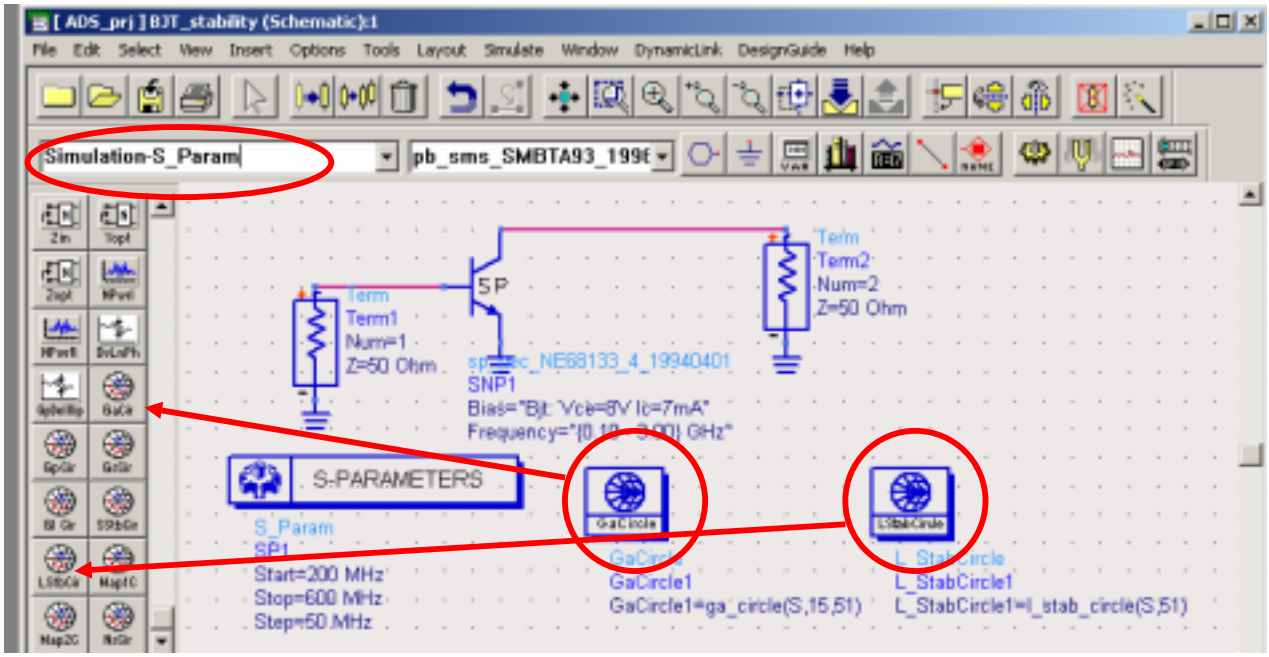
4. For the transistor biasing circuit, Ic and Vce are chosen to be 7mA and 8V respectively. To make 8V Vce, 510 Ohm Rc and 11.57 Vcc are chosen correspondingly. After fixed the Vcc, suitable Vb is needed to make 7mA Ic. As a result, a DC simulation is performed to obtain the proper Vb value.



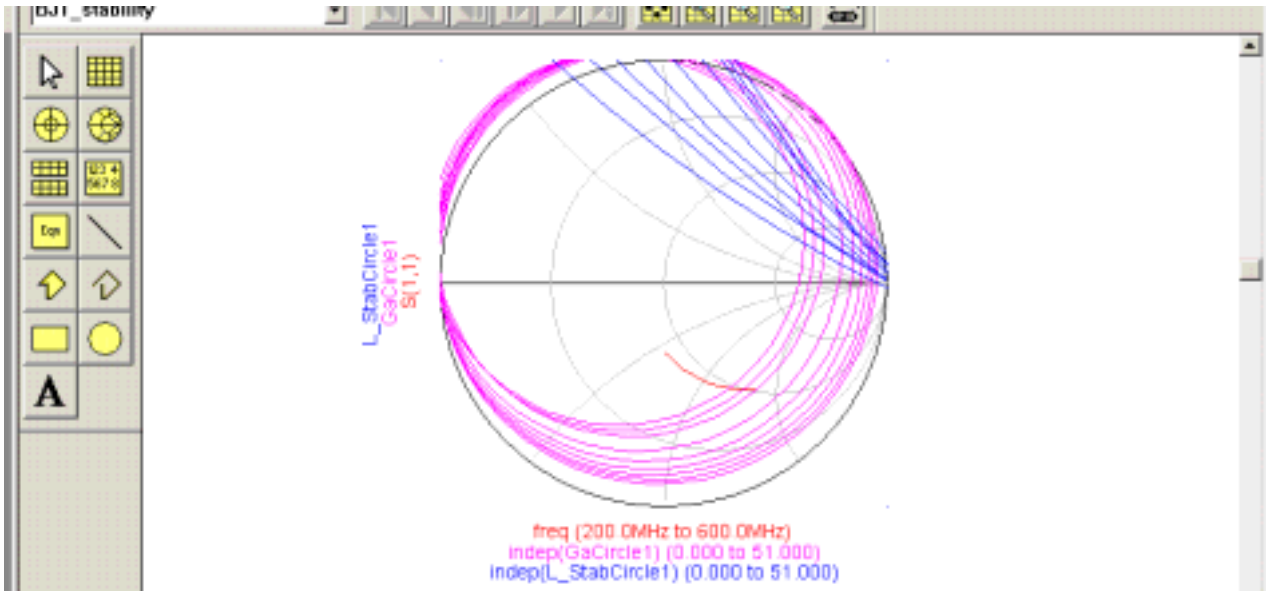
5. From the simulation result, it is known that 0.885 Vb can make the desired Ic value 8mA.



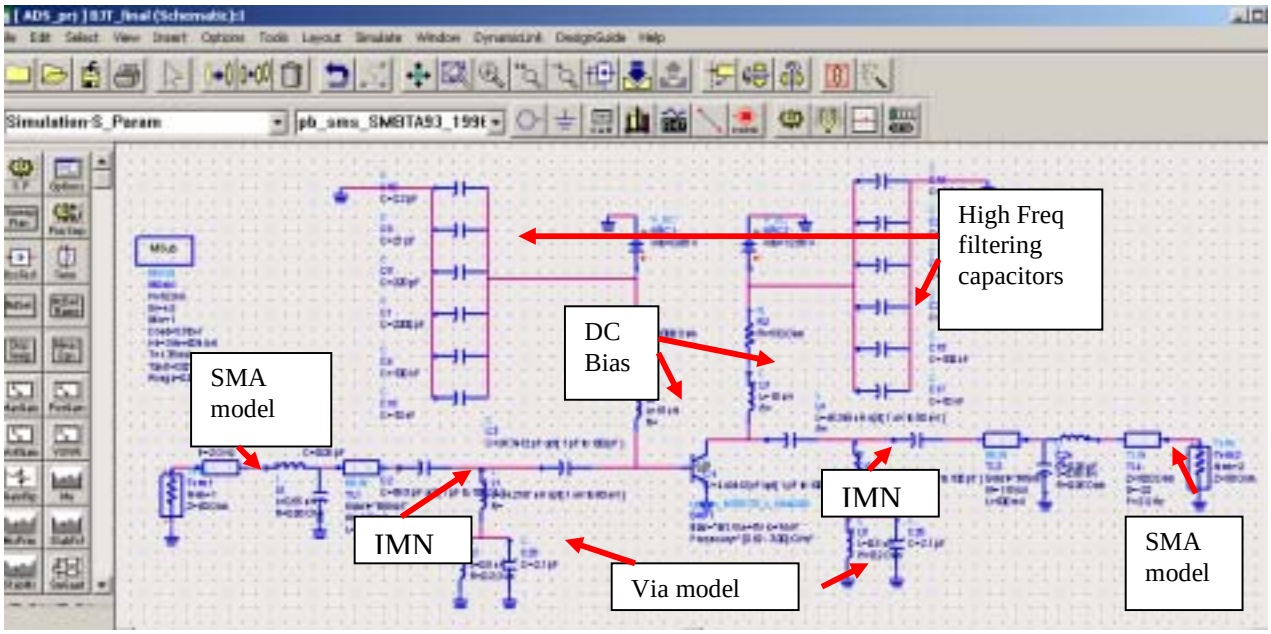
6. After designed the suitable biasing circuit of the chosen transistor, we need to check the stable region, S11 position and gain circles for the bare transistor. After obtaining these parameters, we can then start to design the input impedance matching network. For the S-parameter, simulation, another suitable model is needed to select from the Library List named "sp_nec_NE68133_4_19940401" as shown below. While the "GaCircle" and "L_StabCircle" simulators can be obtained from the "Simulation-S_Param" tag.



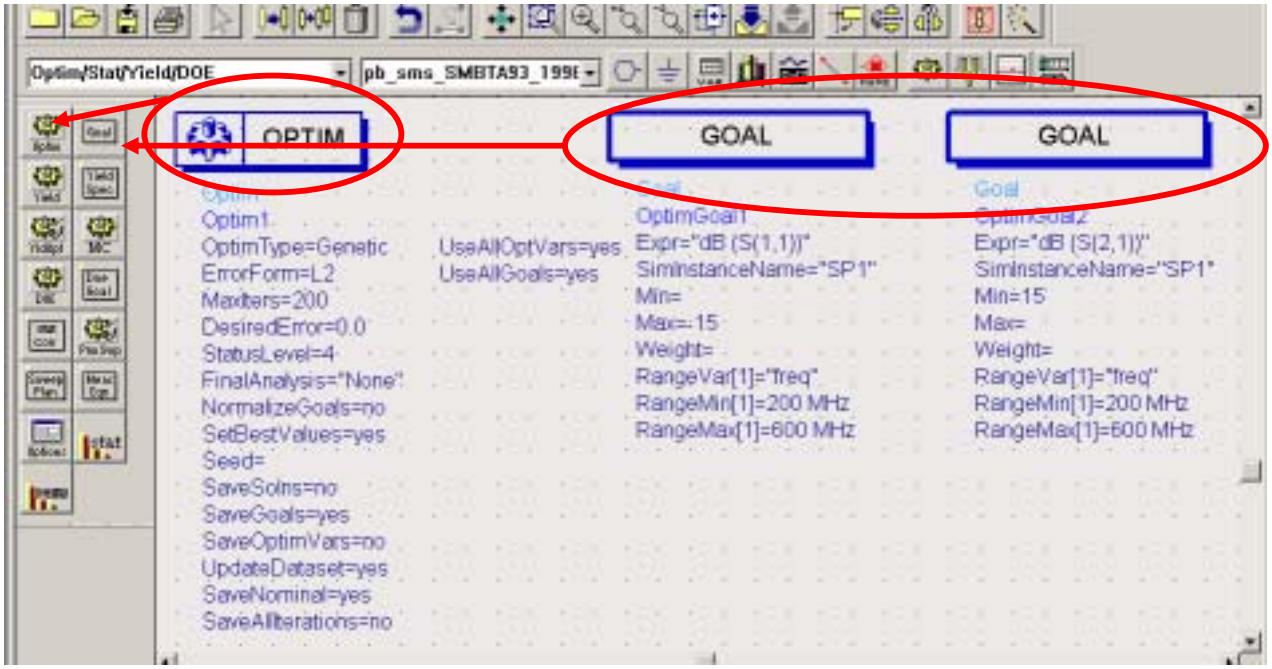
7. The region below the blue lines is stable region. The region within the pink circles is gain circle at 15 dB from 200 to 600 MHz. the red line is the location of S11.



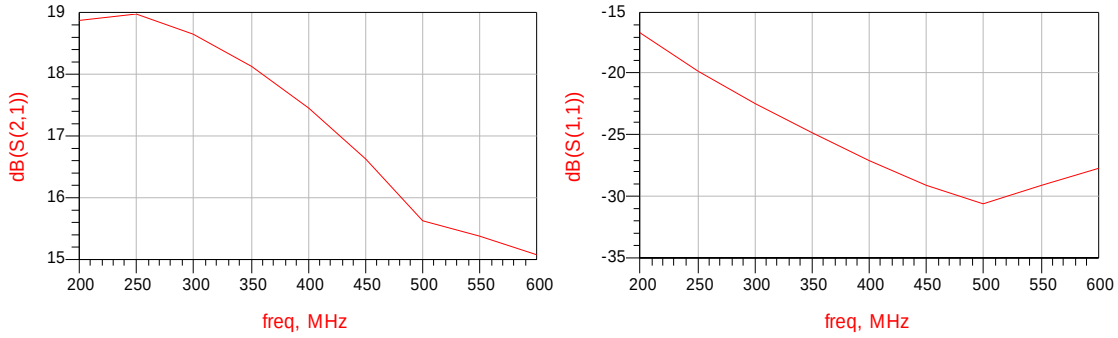
8. Now, we can add the impedance matching network, high frequency filtering capacitors, SMA connector model, via hole model and DC biasing circuit to the transistor to make a single stage amplifier.



9. For the design of impedance matching network, we can use the optimization function provided in ADS to find out the appropriate capacitor and inductor values of the matching networks.



10. The following 2 graphs show the simulated gain and input reflection coefficient of the designed amplifier. You can observe that both of the gain (S21) and input reflection coefficient (S11) fulfill the previous set goals.



Conclusion

The procedures of designing a power amplifier with proper biasing, impedance matching network to meet the specified goals of minimize input reflection coefficient, gain while fulfill the stability requirement are described. It can be seen that with the powerful simulation tool ADS, great design aid is provided to user within the automatic optimization functions in determining the parameters values to meet the specified goals.