ELEC4410 CMOS VLSI Design

Course Description

CMOS process and design rules; MOS device electronics; CMOS circuit and logic circuit characterization and performance estimation; VLSI design and verification tools. Laboratory work will be centered on industry standard tools. *Prerequisite(s):* ELEC 2200 OR ELEC 3310 OR ISDN 4000D

List of Topics

Lecture Topics

1. Course Description
2. Introduction to CMOS VLSI Design
3. MOS Transistor Theory I
4. MOS Transistor Theory II
5. CMOS Combinational Design
6. CMOS Technology, CMOS Layout and Packaging
7. CMOS Inverter DC Characteristics
8. Timing and Dynamic Circuit Characteristics
9. Advanced Design Consideration and Other Design Styles

Lab Topics

1. Unix and Cadence Setup, Schematic Entry
2. Schematic Entry and Circuit Simulation
3. Hierarchical Schematic Design
4. Layout Editor and Design Rule Check
5. Layout Versus Schematic
6. Post-Layout Simulation

Statement of Objectives/Outcomes:

On successful completion of this course, students will be able to:

CO1 – recognize the advantages and critical importance of CMOS technology for very-large-scale integration

CO2 – understand the physical structure and operation of digital CMOS integrated circuits

CO3 – use a computer-aided-design tool for developing and characterizing CMOS integrated circuits

CO4 – design and demonstrate high-performance and compact digital CMOS integrated circuits

CO5 – understand the basic principles and current challenges in CMOS technology scaling

CO6 – foresee the evolution of the integrated circuits technology for the next 10+ years

CO7 – manage small-scale group projects

CO8 – demonstrate effective communication skills

CO9 – understand the professional and ethical responsibilities of engineers.

Textbook(s):
Jan M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits – A Design Perspective*, Second edition, Prentice Hall, 2003

Reference Books/Materials:

1. J. P. Uyemura, *Chip Design for Submicron VLSI: CMOS Layout and Simulation*, Thomson, 2006
2. E. Brunvand, *Digital VLSI Chip Design with Cadence and Synopsys CAD Tools*, Addison-Wesley, 2010

Relationship of Course to Program Outcomes:

Please refer to the Report Section 4.3.2 (iii).

Grading Scheme:

Course Project	15%
Midterm Examination	25%
Final Examination	60%