



Analog Design Engineer

The successful applicant will take part in designing and evaluating current micro-architecture of different major Analog IPs, including high speed SERDES, high performance linear regulator, PLL, etc. and contribute to the various phases of the development work, including but not limited to feasibility studies, performance and functional modeling, design benchmarking, micro-architecture definition. The individual shall work closely with the architects, signal integrity team, physical integration team and product team to deliver best in class Analog IPs design.

Responsibilities

- Generating design specifications and determining micro-architecture for DDR4/5, LPDDR4/5, GDDR6 memory interface PHY IPs, high performance on-die linear regulator and PLL.
- Participating in circuit design and simulation, physical layout design and review of physical design layout of circuits.
- Participating in development of rtl behavioral model, timing model, and system performance model of circuits.
- Participating in evaluation and troubleshooting of circuits.



AI Performance Firmware Engineer

Job Description

- Develop firmware on programmable ASIC chips, make full use of the hardware resource to complete deep learning tasks.
- Develop and debug CNN processor's driver/API/protocol design in Linux environment



Performance Modeling Engineer

The successful applicant will take part in evaluating current micro-architecture of different major functional units of a processor core and contribute to the various phases of the development work, including but not limited to feasibility studies, performance and functional modeling, software benchmarking, micro-architecture definition. The individual shall work closely with the architects and the team to deliver the processor core that meets the requirements of high performance, low power, and scalability for AI application.

Responsibilities

- Interact with the architects, software teams and to evaluate the micro-architecture of the core units including multi-core scheduler, memory hierarchy and various interconnects
- Define verification and validation strategies at different levels for the processor core and carry out the related work to ensure functional correctness and meeting performance targets.



CPU/AI Accelerator Digital Design or Verification Engineer

The successful applicant will take part in defining the micro-architecture of different major functional units of a processor/AI accelerator core and contribute to the various phases of the development work, including but not limited to feasibility studies, cost and power estimation, performance and functional modeling, software benchmarking, micro-architecture definition, front end design and verification, and synthesis.

Responsibilities

- Define the micro-architecture of the Processor/AI Accelerator core including memory hierarchy and various interconnects
- Evaluate and perform trade off analysis of hardware implementation between performance, cost and power.
- Define verification and validation strategies at different levels for the processor/AI Accelerator core and carry out the related work to ensure functional correctness.



Physical Design Engineer/Semi-Custom Physical Design Engineer

Responsibilities

- Design from Gate-level netlist to GDSII (include DFT、FloorPlan、 placement、 CTS、 Routing、 Poweranalysis、 SI analysis、 STA、 Physicalverify、 XRC)
- Support IC design teams for timing closure
- Support pre-maskECO & Post-maskECO
- (Semi-Custom) Focus on structured circuit design, layout, characterization, flow automation and physical design of high-speed and low-power data path subsystems
- (Semi-Custom) Support IP development (physical design, collateral generation, flow development) and PPA quantification
- (Semi-Custom) Support block layout using custom/semi-custom/stdcell libraries
- (Semi-Custom) Support block level floor planning using custom and/or tiling techniques



ASIC Design Engineer

The ASIC Design Engineers will be responsible or take part in defining the micro-architecture of different major functional units of a pipelined processor system. The individual shall be responsible or contribute to the various phase of the development work, including but not limited to feasibility studies, cost and power estimation, performance and functional modeling, micro-architecture definition, front end design and verification, and synthesis. The individual shall work closely with the rest of the team to deliver an SOC that meets the requirements of low cost, low-power, and high performance for wide variety of applications.

Responsibilities

- Verify design by computer simulation and/ or emulation.
- Prepare and maintain block diagram, schematics and components information.
- Oversee and perform layout design, timing analysis and ECO logic changes.
- Evaluate and characterize FPGA/ASIC prototype units.

华为海思图灵业务部 -- 2022 届毕业生招聘活动

工作地：深圳、西安，北京，上海可选。

工作岗位：数字芯片、模拟芯片、算法和软件。

毕业时间：2021.1.1-2022.12.30 毕业的同学。

要求：只要学过数电模电，有电路基础知识的同学都欢迎。（工作岗位描述请参考附件）

申请方法：电邮联系方式（电邮 /WeChat 号）到 mak.ki.leung@huawei.com ,
hungw.wilson@huawei.com, eric.ng@huawei.com 即可。

申请时间：2021.12.31 前

如有问题，[请电邮 hungw.wilson@huawei.com](mailto:hungw.wilson@huawei.com) 或 wechat 查詢



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