

Principal IC Layout Engineer

HONG KONG OR SHENZHEN, FULL-TIME REGULAR

Principal IC layout engineer will be responsible for layout of cutting edge high-speed and/or high-performance BiCMOS/CMOS integrated circuits full chip in deep submicron CMOS processes. The ideal candidate will lead the layout team to finish the full chip layout with passed all necessary checks. Candidate with less experience will be considered as Senior IC layout engineer.

Qualifications

- MS or Bachelor with 8+ years of work experience in high-performance analog/mixed-signal IC layout in deep submicron CMOS or BiCMOS processes
- Track record on successful mass production experience
- Extensive experience with layout of high-performance analog blocks such as analog-to-digital converter, digital-to-analog converter, PLL and precision reference
- Understanding of high-performance analog layout techniques such as common centroid layout, use of dummies, shielding, full of symmetry, matching, and layout consideration for ESD, latchup, electromigration, substrate-noise coupling, crosstalk
- Support analog designers to run EMIR, and aging simulations
- Understanding IO and advanced flip chip packaging techniques
- Work independently according to schedules and be an active team player

Compensations

- 12-month basic salary (above HK600,000 in HK or RMB¥600,000 in SZ), annual bonus, company shares, holidays (all negotiable and depends on qualifications)