

# Principal Digital IC Design Engineer

HONG KONG OR SHENZHEN, FULL-TIME REGULAR

Principal Digital Design Engineer works on high-performance analog-to-digital converter (ADC) and digital-to-analog converter (DAC). The successful candidate in this role will assist engineers in analog/mixed-signal team to develop and verify the digital calibration engine for high-performance data converters. All algorithms are provided by CTO, and you will be responsible for writing RTL, verification, analysis, synthesis, and place-and-route for digital engine in high-performance data converters. AMS will be run by analog leader. This position is open to both RTL code engineers and synthesis engineers, depending on experience and background. The ideal candidate is capable of both pre and post digital designs with higher compensation. Candidate with less experience will be considered as Senior Engineer.

## Qualifications

- MPhil preferred with 5+ year of experience in high-performance digital or mixed-signal IC development in deep submicron CMOS processes
- Understanding of digital design for mixed-signal control loops and writing Verilog code to control and calibrate analog circuits imperfection
- Understanding in multi-clocking design and clock tree architecture
- Understanding of interface such as SPI, LVDS and JESD204B/C standards
- Ability to write full testbenches for verifications in digital (for RTL engineer)
- Familiar with design synthesis tool, and place and route tool (for synthesis engineer)
- Familiar with Cadence Encounter tool (for synthesis engineer)
- Familiar with power analysis, timing closure and static timing analysis tools
- Work independently according to schedules and be an active team player

## Compensations

- 12-month basic salary (above HK700,000 in HK or RMB¥700,000 in SZ), annual bonus, company shares, holidays (all negotiable and depends on qualifications)