

CPU/AI Accelerator Digital Design or Verification Engineer /Intern

The successful applicant will take part in defining the micro-architecture of different major functional units of a processor/AI accelerator core and contribute to the various phases of the development work, including but not limited to feasibility studies, cost and power estimation, performance and functional modeling, software benchmarking, micro-architecture definition, front end design and verification, and synthesis.

Responsibilities

- Define the micro-architecture of the Processor/AI Accelerator core including memory hierarchy and various interconnects
- Evaluate and perform trade off analysis of hardware implementation between performance, cost and power.
- Define verification and validation strategies at different levels for the processor/AI Accelerator core and carry out the related work to ensure functional correctness.

Desired Skills and Experience

BS or higher degree in Electrical/Computer Engineering with knowledge in ASIC design/verification.

Experience with the design/verification in one or more of the following disciplines

- Digital Circuit liked finite state machine and arithmetic circuit design
 - RISC-V CPU
 - FPGA implementation
 - CNN hardware implementation
 - Instruction fetch and dispatch unit
- Load Store Unit
- Execution, Integer and Floating Point Unit
- Good understanding of computer system architecture, memory systems or cache coherency
- Good understanding high speed circuit and low power design is a plus
- Good understanding of TCP/IP networking/service packet protocols is a plus

Interested candidates please apply by sending email to choi.man@huawei.com with your resume.