



# Digital Design / Verification Engineer (Internship)

The eTopus team is comprised of industry experts in high-speed, mixed signal digital signal processing (DSP) communications systems. As a Digital Design / Verification Engineer in eTopus, you will handle all aspects of SoC digital design for networking devices, including micro-architecture definition, system integration, clock domain specification, area and power estimation and DFT architecture definition.

## What can eTopus do for you?

- Potential for upward mobility in a fast-moving Silicon Valley startup.
- Opportunity to work with the like-minded talent to solve challenging problems.
- Becoming part of the creator of ultra-high speed interconnect technology to enable the next generation of Cloud Data Centers.

## What can you do for eTopus?

- Work closely with design, marketing, potential customers and perform SoC micro-architecture definition Intellectual Property (IP) specification & vendor selection and system integration.
- Perform block level RTL coding, chip level integration, including internal and external IPs, and micro-processors.
- Conduct system level functional verification.
- Drive SoC timing closure, DFT, signal integrity and power integrity flow.
- Perform total SoC PPA optimization.

## Required skills and experience

- Multiple Tape-out experience in <40nm process nodes.
- Hands-on experience in RTL coding in Verilog, simulation & synthesis tools, Tcl, Perl, Python and Matlab scripting.
- Hands-on experience with lab equipment.
- Experience with 10G+ networking or communication development a plus.
- Advanced CMOS technologies such as 40nm, 28nm and below.

## Minimum Qualification

- Major in EE, computer engineer or related field
- Strong self-learning ability
- Working location: Hong Kong office / Headquarters & Innovation Center

Apply for this position: [jobs@etopus.com](mailto:jobs@etopus.com)