The Hong Kong University of Science and Technology

UG Course Syllabus

FPGA based Design: From Theory to Practice

ELEC 4320

3 Credits

Pre-requisites: ELEC 2350 or ELEC 3310

Name: Wei Zhang

Email: eeweiz@ust.hk

Office Hours: Tuesday 5-7pm, Rm 2449

Course Description

This course introduces the basic theory and design skills for FPGA-based design. The course aims to equip the students with knowledge and skills for real-world digital system design using FPGA devices. Major topics include an introduction to reconfigurable computing, Verilog hardware description language, FPGA device architecture, mapping flow, and some case studies for the practical system design. Students are expected to gain hands-on experiences in a complete FPGA-based design cycle, from design specification, synthesis, implementation and simulation in this course.

Intended Learning Outcomes (ILOs)

By the end of this course, students should be able to:

1. Know the design flow of FPGA based design, basic architecture of FPGA device

2. Learn the basics of Verilog, a hardware description language (HDL)

3. Learn how to develop RTL design based on Verilog, and implement the design on FPGA

4. Learn the high-level synthesis design flow

5. Know how to analyze the performance of a FPGA based design

Assessment and Grading

This course will be assessed using criterion-referencing and grades will not be assigned using a curve. Detailed rubrics for each assignment are provided below, outlining the criteria used for evaluation.

Assessments:

Assessment Task	Contribution to Overall Course grade (%)	Due date

Homework	20%	3 homeworks, every 3 weeks
Lab	20%	4 labs, starting from week 4
Midterm Examination	30%	Around week 10
Term Project	30%	Presentation in the exam week

* Assessment marks for individual assessed tasks will be released within two weeks of the due date.

Mapping of Course ILOs to Assessment Tasks

Assessed Task	Mapped ILOs	Explanation
Homework	1,2,4,5	This task assesses the student's understanding of FPGA architecture, apply of Verilog in the RTL design, basics of HLS design, evaluation of the design performance, etc.
Lab	2-4	This task gives the students the opportunity to learn the hands-on design on RTL and HLD based design and corresponding implementation flow on FPGA.
Midterm	1-5	There will be open-book midterm exam, it assesses how the students grasp the basic knowledges on the reconfigurable computing, FPGA architecture, RTL and HLS based design.
Term project	2-5	It will be an extension of the labs, and evaluate the students' hands-on design skills.

Grading Rubrics

We will grade based on the following.

- Correctness and quality of the answer for the midterm exam and homework
- Design quality, novelty and overall efforts of each team member for the term project
- There is penalty if it is a late submission

Final Grade Descriptors:

Grades	Short Description	Elaboration on subject grading description
A	Excellent Performance	Students in the course demonstrate a strong grasp of lecture materials, excellent in problem-solving, expertise in the digital design, effectively utilize tools discussed, excel in laboratory experiments, and excel in various project stages.

B	Good Performance	Students exhibit a solid understanding of lecture materials, proficient use of tools, competence in problem-solving, satisfactory completion of laboratory experiments and term project.
C	Satisfactory Performance	Possesses adequate knowledge of core subject matter, competence in dealing with familiar problems, satisfactory use of tools, and completion of laboratory experiments, acceptable progress of term project.
D	Marginal Pass	Has threshold knowledge of core subject matter, potential to achieve key professional skills, and the ability to finish the minimum requirement of lab and term project.
F	Fail	Insufficient understanding of the subject matter and lacks the necessary problem-solving skills. Fail to finish the minimum requirement of labs and term project.

Course AI Policy

The use of Generative AI in project is permitted with proper acknowledgement and will NOT be contributed to the students' work.

Communication and Feedback

Assessment marks for individual assessed tasks will be communicated via Canvas within two weeks of submission. Feedback on assignments will include specific details, e.g., what is wrong and areas for improvement. Students who have further questions about the feedback, including marks should consult the TA or instructor within five working days after the feedback is received.

Resubmission Policy

To ensure fairness for students who submit assignments on time, a penalty for late submission is listed as follows:

- Late submission within 12 hours, 15% penalty will be applied.
- Late submission between 12 to 24 hours, 30% penalty will be applied.
- Late submission between 24 to 48 hours, 50% penalty will be applied.
- Late submission for more than 48 hours will not be accepted.

Required Texts and Materials

No specific Textbook, mainly based on course slides. Additional tutorial and reading materials will be provided.

Academic Integrity

Students are expected to adhere to the university's academic integrity policy. Students are expected to uphold HKUST's Academic Honor Code and to maintain the highest standards of academic integrity. The University has zero tolerance of academic misconduct. Please refer to Academic Integrity | HKUST – Academic Registry for the University's definition of plagiarism and ways to avoid cheating and plagiarism.