**The Hong Kong University of Science and Technology**

**UG Course Syllabus**

**Digital Fundamentals and System Design [Fall 2024/25]**

ELEC3310

4 credits

Exclusion(s): ELEC 2200, ISDN 4000D

Prerequisite(s): ELEC 1100

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**Office Hours:** Tue & Thu 11:00am - 12:00pm, Room 3102 (CYT)

**Course Description**

Design and synthesis of digital circuits with main emphasis on sequential logic taught through project-based learning approach. Laboratory assignments make extensive use of VHDL and FPGAs and prepare students for an open-ended project undertaken in the remaining part of the course.

**Intended Learning Outcomes (ILOs)**

By the end of this course, students should be able to:

ILO1 – Describe and analyze sequential logic circuits.

ILO2 – Design, model, and simulate sequential logic circuits using register-transfer level (RTL) design abstractions and hardware description languages (HDL).

ILO3 – Design, implement, and test sequential circuits and systems using field-programmable gate arrays (FPGAs).

ILO4 – Develop a model engineering system following a hierarchical design principle.

**Assessment and Grading**

This course will be assessed using criterion-referencing and grades will not be assigned using a curve. Details are provided below.

**Assessments:**

| Assessment Task | Contribution to Overall Course grade (%) | Due date |
|---|---|---|
| Homework | 0%<br>(*Homework assignments will be graded and taken into consideration when further reference is needed about the student performance)* | Week 3 to Week 13 |
| Laboratory | 25% | Week 4 to Week 13 |
| Project | 15% | Week 13 |
| Mid-Term Examination | 25% | Week 7 |
| Final Examination | 35% | Week 15 to Week 16 |

**Mapping of Course ILOs to Assessment Tasks**

| Assessed Task | Mapped ILOs | Explanation |
|---|---|---|
| Homework | ILO1, ILO4 | This task assesses students' ability to describe and analyze sequential logic circuits (IL01), and to design and develop a model engineering system following hierarchical design principle (IL04). |
| Laboratory & Project | IL02, ILO3, IL04 | This task enriches students' knowledge in designing sequential logic circuits using HDL (IL02), developing a hierarchical design principle (IL04) and implementing & testing them using FPGA (IL03). |
| Mid-Term & Final Examination | IL01, IL02, L03 | Mid-Term & Final exams are designed to assess students' understanding of combinational & sequential logic circuits (ILO1), their design using RTL design abstractions and HDL (IL02), and their implementation using FPGAs (IL03). |

**ELEC3310 Project Grading Rubric**

| Marks | Excellent | Good | Satisfactory | Marginal | Fail |
|---|---|---|---|---|---|
| **Minimized state diagram & state table**<br><br>**Max: 10%** | Demonstrates excellent understanding of FSM design from the lecture & tutorial materials | Demonstrates a solid understanding of FSM design from the lecture & tutorial materials | Demonstrates an adequate understanding of FSM design from the lecture & tutorial materials | Demonstrates a limited understanding of FSM design from the lecture & tutorial materials | Demonstrates a lack of understanding of FSM design from the lecture & tutorial materials |
| **Simulation Test ***<br><br>**Max: 35%** | Demonstrates exceptional understanding on how to represent and simulate a digital system using VHDL. | Demonstrates a strong understanding on how to represent and simulate a digital system using VHDL. | Demonstrates a satisfactory understanding on how to represent and simulate a digital system using VHDL. | Demonstrates a basic understanding on how to represent and simulate a digital system using VHDL. | Demonstrates minimal understanding on how to represent and simulate a digital system using VHDL. |
| **Board Test ***<br><br>**Max: 40%** | Demonstrates exceptional understanding on how to create Design Constraints for the Basys3 Board and how to program it for testing. | Demonstrates a strong understanding on how to create Design Constraints for the Basys3 Board and how to program it for testing. | Demonstrates a satisfactory understanding on how to create Design Constraints for the Basys3 Board and how to program it for testing. | Demonstrates a basic understanding on how to create Design Constraints for the Basys3 Board and how to program it for testing. | Demonstrates minimal understanding on how to create Design Constraints for the Basys3 Board and how to program it for testing. |
| **Block diagram Design & description**<br><br>**Max: 15%** | Shows excellent understanding of structural modeling and the use of digital hardware components learned in class & tutorials | Shows a solid understanding of structural modeling and the use of digital hardware components learned in class & tutorials | Shows an adequate understanding of structural modeling and the use of digital hardware components learned in class & tutorials | Shows a limited understanding of structural modeling and the use of digital hardware components learned in class & tutorials | Shows a lack of understanding of structural modeling and the use of digital hardware components learned in class & tutorials |

* Remarks: If students don't submit all the Vivado files (VHDL, testbench, etc.) required in the project they will get marks deducted.

**Final Grade Descriptors:**

| Grades | Short Description | Elaboration on subject grading description |
|---|---|---|
| A | Excellent Performance | Students with excellent performance in the course demonstrate a strong grasp of the lecture & tutorial materials, effectively utilizing the tools discussed, excel in laboratory experiments and the project, and to be able to design digital circuits using logic gates and HDL. |
| B | Good Performance | Students with good performance in the course exhibit a solid understanding of the lecture & tutorial materials, proficient use of tools discussed, and competent completion of laboratory experiments & the project. They showcase commendable knowledge and skills to design digital circuits using logic gates and HDL. |
| C | Satisfactory Performance | Students with satisfactory performance demonstrate an adequate understanding of the lecture & tutorial materials, satisfactory use of tools discussed, and completion of laboratory experiments & the project. They showcase satisfactory knowledge and skills to design digital circuits using logic gates and HDL. |
| D | Marginal Pass | Students with marginal pass show limited understanding of the lecture & tutorial materials, inconsistent use of tools discussed, and incomplete or inconsistent performance in the laboratory experiments & the project. They exhibit limited skills to design digital circuits using logic gates and HDL. |
| F | Fail | Students who fail the course display a lack of understanding of the lecture & tutorial materials, inadequate use of tools, and unsuccessful completion of some of the laboratory experiments & the project. They lack the skills to design digital circuits using logic gates and HDL. |

**Course AI Policy**

The use of Generative AI in homework assignments, laboratory experiments and the project is permitted with proper acknowledgement.

**Communication and Feedback**

Assessment marks & feedback for individual assessed tasks will be communicated via Canvas within two weeks of submission. Students who have further questions about the feedback including marks should consult the instructor, Teaching Associate or PGTAs within one week after the feedback is received.

**Resubmission Policy**

We will accept resubmission of homework assignments, lab reports and project report ONLY if they are resubmitted through Canvas BEFORE the announced due-date. **We will NOT ACCEPT late submissions**.

**Required Texts and Materials (Textbook & Notes)**

Title: Digital Fundamentals, Global Edition, 11th Edition
Author: Thomas L Floyd
Print Book ISBN: 9781292075983

Lecture notes and Tutorial notes will be provided.

**Academic Integrity**

Students are expected to adhere to the university's academic integrity policy. Students are expected to uphold HKUST's Academic Honor Code and to maintain the highest standards of academic integrity. The University has zero tolerance of academic misconduct. Please refer to Academic Integrity | HKUST – Academic Registry for the University's definition of plagiarism and ways to avoid cheating and plagiarism.

**Additional Resources (Reference Books/Materials):**

Title: Digital Design, Global Edition, 6th Ed
Author: M. Morris Mano & Michael D. Ciletti
ISBN: 9781292231167