**The Hong Kong University of Science and Technology**

**UG Course Syllabus**

**Practical Considerations of Analog Integrated Circuit Design**

ELEC4450

3 Credits

Pre-requisites: ELEC3400

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**Office Hours:** By email appointments and using Zoom

**Course Description**

The performance of analog integrated circuits is fundamentally tied to the behavior of key building blocks, such as current mirrors and differential pairs. These components depend critically on the matching properties of paired MOSFETs. In advanced CMOS technology, these properties are influenced not only by channel width and length but also by layout-dependent effects and parasitic elements unique to scaled processes. This course explores the impact of these phenomena on analog circuit behavior, equipping students with practical methodologies to mitigate their influence and optimize circuit design.

**Intended Learning Outcomes (ILOs)**

By the end of this course, students should be able to:

1. Understand the layout view and cross-sectional view of deeply scaled PMOSFETs, NMOSFETs, and isolated-NMOSFET.
2. Identify parasitic components in deeply scaled CMOS technologies and understand their impact on analog circuit performance.
3. Understand the impact of short-channel effects, layout dependent effects, and process variations, on analog circuit performance.
4. Analyze and compute the impact of process variations on analog circuit performance such as accuracy of a current mirror and input offset voltage of an amplifier.
5. Apply various design and layout methodologies to minimize the impact of short-channel effects, layout dependent effects, and process variations, on analog circuit performance.
6. Apply industry software, Cadence, to design analog circuits and evaluate their performance under the impact of short-channel effects, layout dependent effects, and process variations.

**Assessment and Grading**

This course will be assessed using criterion-referencing and grades will not be assigned using a curve. Detailed rubrics for each assignment are provided below, outlining the criteria used for evaluation.

**Assessments:**

| Assessment Task | Contribution to Overall Course grade (%) | Due date |
|---|---|---|
| Lab 1 Report | 6% | Week 7 |
| Lab 2 Report | 12% | Week 10 |
| Lab 3 Report | 12% | Week 12 |
| Project Report | 35% | Week 13 |
| Final Examination | 35% | Assigned examination date |

**Mapping of Course ILOs to Assessment Tasks**

| Assessed Task | Mapped ILOs | Explanation |
|---|---|---|
| All Labs | ILO3, ILO4, ILO5, ILO6 | Provides students with hands-on experience using industry software (Cadence) to explore and address key challenges (e.g., short-channel effects, layout dependent effects, process variations) in analog integrated circuit design. |
| Project Report | ILO3, ILO4, ILO5, ILO6 | Evaluates students' ability to apply course knowledge and skills in designing and optimizing analog integrated circuits, including the proficient use of industry software (Cadence) for circuit design and performance evaluation |
| Final Examination | ILO1, ILO2, ILO3, ILO4, ILO5 | Tests comprehensive understanding and analytical skills across all topics covered in this course. |

**Grading Rubrics**

| Task | Excellent Performance | Good Performance | Satisfactory Performance | Marginal Pass | Fail |
|---|---|---|---|---|---|
| All Labs | Demonstrates deep understanding of MOSFET matching properties and exceptional skills in solving key analog design challenges | Shows strong understanding of MOSFET matching properties and effective skills in solving key analog design challenges | Demonstrates basic understanding of MOSFET matching properties and basic skills in solving key analog design challenges | Displays minimal understanding of MOSFET matching properties and struggles in solving key analog design challenges | Lack understanding of MOSFET matching properties and not able to solve key analog design challenges |

| | | | | | |
|---|---|---|---|---|---|
| Project Report | Demonstrates outstanding design methodologies to achieve analog circuit performance requirements by comprehensively mitigating all effects present in scaled CMOS technology. | Applies effective design methodologies to achieve analog circuit performance requirements by mitigating major effects present in scaled CMOS technology. | Demonstrates basic design methodologies to meet essential analog circuit performance requirements, while addressing some effects present in scaled CMOS technology. | Shows limited ability in applying design methodologies, with partial achievement of analog circuit performance requirements and minimal consideration of effects present in scaled CMOS technology. | Demonstrates unsatisfactory design methodologies, with inability to meet analog circuit performance requirements or address the effects present in scaled CMOS technology. |
| Final | Demonstrates comprehensive understanding and analysis of all course topics | Shows strong understanding and analysis of major course topics | Exhibits satisfactory understanding and analysis of core course topics such as process variations and mismatch properties of paired MOSFETs | Displays minimal understanding and analysis of course topics related to practical analog integrated circuit design | Lacks understanding and analysis of course topics related to practical analog integrated circuit design |

**Final Grade Descriptors:**

| Grades | Short Description | Elaboration on subject grading description |
|---|---|---|
| A | Excellent Performance | Demonstrates a comprehensive grasp of subject matter, expertise in problem-solving, and significant creativity in thinking. Exhibits a high capacity for scholarship and collaboration, going beyond core requirements to achieve learning goals. |
| B | Good Performance | Shows good knowledge and understanding of the main subject matter, competence in problem-solving, and the ability to analyze and evaluate issues. Displays high motivation to learn and the ability to work effectively with others. |
| C | Satisfactory Performance | Possesses adequate knowledge of core subject matter, competence in dealing with familiar problems, and some capacity for analysis and critical thinking. Shows persistence and effort to achieve broadly defined learning goals. |
| D | Marginal Pass | Has threshold knowledge of core subject matter, potential to achieve key professional skills, and the ability to make basic judgments. Benefits from the course and has the potential to develop in the discipline. |
| F | Fail | Demonstrates insufficient understanding of the subject matter and lacks the necessary problem-solving skills. Shows limited ability to think critically or analytically and exhibits minimal effort towards achieving learning goals. Does not meet the threshold requirements for professional practice or development in the discipline. |

**Course AI Policy**

Use of generative artificial intelligence tools is allowed provided that the use is declared.

**Communication and Feedback**

Assessment marks for individual assessed tasks will be communicated via Canvas within three weeks of submission. Students who have further questions about the feedback including marks should consult the instructor within five working days after the feedback is received.

**Late Submission Policy**

All assignments have to be submitted through the Canvas course website. Any late submission will immediately receive a 20% mark deduction, and additional 20% mark deduction will be applied for each additional 24 hours of late. Timestamp recorded by the Canvas course website is used to determine how late your submission is.

**Required Texts and Materials**

Lecture notes will be available on the Canvas course webpage.

**Academic Integrity**

Students are expected to adhere to the university's academic integrity policy. Students are expected to uphold HKUST's Academic Honor Code and to maintain the highest standards of academic integrity. The University has zero tolerance of academic misconduct. Please refer to Academic Integrity | HKUST – Academic Registry for the University's definition of plagiarism and ways to avoid cheating and plagiarism.

**Additional Resources**

- Alan Hastings, *The Art of Analog Layout (2nd edition)*, Pearson Prentice Hall, 2006
- Short Course from Prof. PE Allen
- gm/id note from Prof. Bernhard Boser