The Hong Kong University of Science and Technology

UG Course Syllabus

CMOS VLSI Design

ELEC 3410

3 Credits

Pre-requisite: ELEC 2400

Name: Khawar Sarfraz

Email: eesarfraz@ust.hk

Office Hours: Mondays, 11:00am-12:00noon

Course Description

This course introduces students to the fundamentals of digital integrated circuits. Topics include MOS transistor theory, CMOS fabrication flow, dc and transient characteristics of CMOS inverter, CMOS power, combinational circuit design and the logical effort approach, CMOS logic families, interconnects, and sequential circuit design. Students will gain hands-on experience with Cadence industry-standard EDA tools to perform labs and later to design, simulate, layout, and verify a small-scale circuit using TSMC's commercial 180nm CMOS technology. In addition to theory, emphasis is placed on best design practices followed in the industry to prepare students for careers in chip design.

Intended Learning Outcomes (ILOs)

By the end of this course, students should be able to:

1. ILO1 – Understand and explain the fundamental principles of CMOS technology including its structure and operation

2. ILO2 – Develop skills to design basic CMOS combinational and sequential circuits according to the most modern industrial practices

3. ILO3 – Analyze and simulate circuit parameters e.g. delay, power, area, noise margins etc.

4. ILO4 – Gain skills in creating and understanding efficient circuit designs and layout with industry-standard CAD tools and a commercial PDK

5. ILO5 – Discuss the impact of scaling on CMOS technology and identify current trends in VLSI design and fabrication

6. ILO6 – Develop skills in teamwork, communication, and problem-solving through a collaborative project

7. ILO7 – Appreciate the ethical and professional responsibilities of engineers

Assessment and Grading

This course will be assessed using criterion-referencing and grades will not be assigned using a curve. Detailed rubrics for each assignment are provided below, outlining the criteria used for evaluation.

Assessments:

Assessment Task	Contribution to Overall Course grade (%)	Due date
Course Project	20%	01/12/2026 *
Labs (7 in total)	14%	24/09/2026 – 12/11/2026 *
Mid-term Examination	30%	16/10/2026 *
Final examination	35%	19/12/2016 *
SFQ Submission	1%	05/12/2026

* Assessment marks for individual assessed tasks will be released within two weeks of the due date.

Mapping of Course ILOs to Assessment Tasks

Assessed Task	Mapped ILOs	Explanation
Course Project	ILO2, ILO3, ILO4, ILO6, ILO7	The project aims to bridge theory with practice. Its purpose is to apply knowledge in a realistic context, to develop hands-on skills, to learn and appreciate the capabilities of the EDA tools, to encourage problem-solving, to prepare students for research and industry roles, and to foster collaboration and communication.
Labs (7 in total)	ILO3, ILO4	The labs are specifically designed to reinforce core concepts and to develop proficiency with the industry-standard Cadence EDA tools.
Mid-term Examination	ILO1, ILO2, ILO3, ILO5, ILO7	The midterm exam is a closed-book, closed-notes assessment. No electronic devices, other than a calculator, are allowed. Based on real-world design problems, this assessment examines students' understanding of MOSFET theory, CMOS fabrication flow, and DC characteristics of an inverter.
Final examination	ILO1, ILO2, ILO3, ILO5, ILO7	The final exam is a closed-book, closed-notes assessment. No electronic devices, other than a calculator, are allowed. Based on real-world design problems, this assessment examines students' understanding of CMOS dynamic characteristics, trade-offs associated with different CMOS logic families, interconnects, logical effort approach to gate sizing, CMOS power, and sequential circuits.

Grading Rubrics

- The midterm and final exam will be graded based on the accuracy of the answers, the correctness of calculations, and the logical progression of steps, with the goal of accurately reflecting students' understanding of the subject matter.
- Lab grades will be assigned based on the completion of the tasks and correct answers to questions within the duration of the lab. Late submissions will not be entertained.
- For the course project, grading will be based on understanding and interpretation of the problem, quality of the implemented design (power, performance, area), degree of completeness, individual student workload and contribution, performance of students in the Q&A session during project demonstration, and the final project report.

Final Grade Descriptors:

[As appropriate to the course and aligned with university standards]

Grades	Short Description	Elaboration on subject grading description
A	Excellent Performance	Demonstrates outstanding understanding of digital integrated circuits, strong technical proficiency with EDA tools, and exceptional performance on the course project, labs, and the midterm/final exam.
B	Good Performance	Shows solid comprehension of course material, competent application of design methodologies, and reliable project execution with minor gaps in depth or precision.
C	Satisfactory Performance	Meets minimum expectations, with adequate but limited understanding of CMOS VLSI design principles and moderate success in applying tools and techniques.
D	Marginal Pass	Reflects significant weaknesses in grasping core concepts with inconsistent or an incomplete course project and labs.
F	Fail	Indicates insufficient understanding or inability to meet course requirements, i.e. on the midterm/final exam, the labs, and the execution of course project.

Course AI Policy

Since AI-assisted design is becoming part of industry practice, students are therefore permitted to experiment with these tools. Students must, however, validate and refine AI-generated outputs to ensure correctness and compliance with the given design specifications. Raw AI generated outputs will not be accepted in any form. Students will also be required to document where and how AI tools were used during the duration of the course.

Communication and Feedback

Assessment marks for individual and group-assessed tasks will be communicated via Canvas within two weeks of submission. Students who have further questions about the feedback including marks should consult the instructor within five working days after the feedback is received.

Resubmission Policy

Late submissions will not be entertained. Students who submit the course project report and labs after the given deadline will not get any points.

Required Texts and Materials

All course material will be available on the Canvas course page.

Academic Integrity

Students are expected to adhere to the university's academic integrity policy. Students are expected to uphold HKUST's Academic Honor Code and to maintain the highest standards of academic integrity. The University has zero tolerance of academic misconduct. Please refer to Academic Integrity | HKUST – Academic Registry for the University's definition of plagiarism and ways to avoid cheating and plagiarism.

[Optional] Additional Resources

Links to reference material will also be available on the Canvas course page.