ELEC4320 FPGA based Design: From Theory to Practice

Course Description

This course introduces the basic theory and design skills for FPGA -based design. The course aims to equip the students with enough knowledge and skills for the real word engineering using FPGA devices. Major topics include introduction to reconfiguable computing, hardware description language, FPGA device, and mapping flow. Students will gain hands-on experiences of the complete FPGA based design cycle, from design specification, synthesis, implementation and simulation in this course.
Prerequisite(s): ELEC 2350

Delivery Mode

By default, the course will be offered in face-to-face mode including the lecture and lab. If there is special request that some student cannot travel to Hong Kong due to restriction, we will consider supporting mixed-mode delivery.

List of Topics

Lecture Topics

Week 1	Introduction of reconfigurable computing concept and basic synthesis flow on FPGA
Week 2	Introduction of Verilog language and basic Verilog syntax
Week 3	More syntax and semantics on Verilog using design examples
Week 4	Reconfigurable device about simple and complex programmable logic devices (PLDs)
Week 5	Introduce FPGA overall structure; Detailed discussion on configurable logic blocks
Week 6	FPGA interconnect architecture and on-chip coarse-grain resources including BRAM, DSP, clock control, etc.
Week 7	Mapping flow for FPGA implementation; Introduce technology mapping algorithm
Week 8	Introduce the placement and routing algorithms for FPGA implementation
Week 9	Design flow for the design using system generator and Matlab Simulink
Week 10	Design flow for high-level synthesis, using C as input language and Vivado synthesis tool
Week 11	In-class Midterm Exam
Week 12	Design flow for system-level design with embedded hard/soft processor core together with FPGA co-processor
Week 13	Case study of some representative design

Lab Topics

1. Xilinx FPGA – Introductory Lab

2. XIlinx FPGA – Digital piano
3. Xilinx FPGA – Simple Microprocessor
4. XIlinx FPGA - Matrix multiplication in high level synthesis

Statement of Objectives/Outcomes:

CO1 - Understand the basic structure and parameters of the FPGA device

CO2 - Understand the operation performed in each step of the mapping flow and its basic algorithm

CO3 - Use the hardware description language (HDL) to describe the logic design

CO4 - Apply FPGA CAD tools to synthesize and implement HDL based design on FPGA

CO5 - Understand the flow for high-level synthesis and apply high-level synthesis to simple design

CO6 - Analyze the design delay and resource usage, further improve the design if needed

Textbook(s):
Lecture notes

Reference Books/Materials:
1. The Verilog® Hardware Description Language
2. Advanced FPGA Design: Architecture, Implementation, and Optimization
3. Xilinx user guide

Grading Scheme:

Homework	20%
Lab Reports	20%
Midterm Examination	30%
Term Project	30%